Claims

1. A single semiconductor element, in particular a diode or transistor, in a flip chip construction, comprising at least
   - a substrate layer (13) at a rear side (11) of the single semiconductor element;
   - an active layer (15, 21) which is arranged between the substrate layer and a contact side (23) of the single semiconductor element disposed opposite the rear side; and
   - at least two solder contacts (29) which are electrically connected to the active layer and project beyond the contact side (23) of the single semiconductor element in order to make possible a direct soldering of the single semiconductor element to a carrier board,

   wherein the contact side (23) is provided with a glass passivation layer (27) which peripherally surrounds the solder contacts (29).

2. A single semiconductor element in accordance with claim 1, wherein the glass passivation layer (27) is interrupted in the region of the solder contacts (29) and in the region of a dividing grid between single semiconductor elements produced adjacently.

3. A single semiconductor element in accordance with claim 1, wherein an oxide layer (25) is provided between the glass passivation layer (27) and the active layer (15, 21).

4. A single semiconductor element in accordance with claim 1, wherein that the solder contacts (29) are connected to the active layer (15, 21) via an intermediate metal layer (31).

5. A method for producing a single semiconductor element in accordance with claim 1 in a flip chip construction,
the method comprising the steps of:
- providing a substrate layer (13) with an active layer (15, 21);
- electrically connecting the active layer to at least two solder contacts (29) which project beyond a contact side (23) of the single semiconductor element; and
- providing the contact side (23) of the single semiconductor element before or after the production of the solder contacts with a glass passivation layer (27) which peripherally surrounds the solder contacts (29),

the step of providing the contact side (23) with a glass passivation layer (27) comprising the sub-steps of:
- wetting the contact side (23) with a suspension such that glass particles contained therein are deposited at the contact side due to gravity or to a centrifugal force; and
- subsequently heating the contact side (23) in order to fuse the deposited glass particles.

6. A method in accordance with claim 5, wherein
the contact side (23) of the single semiconductor element is first provided with the glass passivation layer (27) over the whole area and the glass passivation layer is then structured photolithographically, with the contact side (23) being liberated from the

glass passivation layer in particular in the region of the solder contacts (29).

7. A method in accordance with claim 5,
wherein the single semiconductor element is produced together with a plurality of other single semiconductor elements on the basis of a common substrate, wherein
- the contact sides (23) of the single semiconductor elements are kept free or liberated from the glass passivation layer (27) along a dividing grid; and
- the single semiconductor elements are sawn apart along the dividing grid.

8. A single semiconductor element, in particular a diode or a transistor, in a flip chip construction, in particular in accordance with claim 1, at least comprising
- a substrate layer (13) at a rear side (11) of the single semiconductor element;
- an active layer (15, 21) which is arranged between the substrate layer and a contact side (23) of the single semiconductor element disposed opposite the rear side; and
- at least two solder contacts (29) which are electrically connected to the active layer and project beyond the contact side (23) of the single semiconductor element in order to make possible a direct soldering of the single semiconductor element to a carrier board;

wherein at least one side face (33) of the single semiconductor element is at least partly provided with an insulator layer (25) for the

avoidance of short circuits on the soldering of the single semiconductor element to the carrier board.

9. A single semiconductor element in accordance with claim 8, wherein at least a quarter, in particular a third, and preferably a half of the side face (33) of the single semiconductor element adjoining the contact side (23) is provided with the insulator layer (25).

10. A single semiconductor element in accordance with claim 8, wherein the side face of the single semiconductor element is completely provided with the insulator layer (25).

11. A single semiconductor element in accordance with claim 8, wherein the single semiconductor element has a mesa construction with lateral etched and sawn through trenches (33), with the respective side face being provided with the insulator layer (25) down to the depth of the respective trench.

12. A single semiconductor element in accordance with claim 8, wherein at least the side faces (33) of the single semiconductor element which respectively directly adjoin a solder contact (29) are provided with the insulator layer (25);
wherein in particular all side faces of the single semiconductor element are provided with the insulator layer (25).

13. A single semiconductor element in accordance with claim 8, wherein the contact side (23) is also provided with the insulator layer (25).

14. A single semiconductor element in accordance with claim 8, wherein the insulator layer is an oxide layer (25).

15. A method for producing a plurality of single semiconductor elements in accordance with claim 8, wherein

- for the preparation of a plurality of adjacent single semiconductor elements, a substrate (13) is provided with a respective active layer (15, 21) and with dividing trenches (33) lying therebetween;
- the active layers (15, 21) and the dividing trenches (33) lying therebetween are provided with an insulator layer (25); and
- the adjacent single semiconductor elements are sawn apart along the dividing trenches (33).

16. A method in accordance with claim 15, wherein the insulator layer is an oxide layer (25).

17. A method in accordance with claim 15, wherein the insulator layer (25) is applied in a CVD process.

18. A single semiconductor element, in particular a diode or a transistor, in a flip chip construction, in particular in accordance with claim 1, at least comprising

- a substrate layer (13) at a rear side (11) of the single semiconductor element;
- an active layer (15, 21) which is arranged between the substrate layer and a contact side (23) of the single semiconductor element disposed opposite the rear side; and

- at least two solder contacts (29) which are electrically connected to the active layer and project beyond the contact side (23) of the single semiconductor element in order to make possible a direct soldering of the single semiconductor element to a carrier board;

wherein the solder contacts (29) have different outlines at the contact side (23) of the single semiconductor element.

19. A single semiconductor element in accordance with claim 18, wherein the shape of the respective outline of the two solder contacts (29) is different.

20. A single semiconductor element in accordance with claim 18, wherein each of the two solder contacts (29) takes up the same area at the contact side (23).

21. A single semiconductor element in accordance with claim 18, wherein each of the two solder contacts (29) has the same peripheral length at the contact side (23).

22. A single semiconductor element in accordance with claim 18, wherein, with the same shape of the respective outline, the area of the two solder contacts (29) taken up in each case at the contact side (23) is different.

23. A single semiconductor element in accordance with claim 18, wherein at least one dummy contact is provided in addition to the two solder contacts (29) to increase the standing stability.

24. A single semiconductor element in accordance with claim 18, wherein at least one of the two solder contacts (29) is made in a plurality of parts at the contact side (23) of the single semiconductor element.

25. A single semiconductor element in accordance with claim 18, wherein at least one of the two solder contacts (29) extends along at least one, preferably along two or three, outer edges of the contact side (23) of the single semiconductor element.

26. A single semiconductor element in accordance with claim 18, wherein one of the two solder contacts (29) has a circular outline and the other of the two solder contacts (29) has an elongate outline; and
wherein the two solder contacts each take up the same area or each have the same peripheral length at the contact side (23).

27. A single semiconductor element in accordance with claim 18, wherein one of the two solder contacts (29) has a U-shaped or C-shaped outline and extends along three outer edges of the contact side (23) of the single semiconductor element; and
wherein the other of the two solder contacts (29) is at least partly enclosed inside the U or C shape of the one solder contact.

28. A single semiconductor element, in particular a diode or a transistor, in a flip chip construction, in particular in accordance with claim 1, at least comprising

- a substrate layer (13) at a rear side (11) of the single semiconductor element;
- an active layer (15, 21) which is arranged between the substrate layer and a contact side (23) of the single semiconductor element disposed opposite the rear side; and
- at least two solder contacts (29) which are electrically connected to the active layer and project beyond the contact side (23) of the single semiconductor element in order to make possible a direct soldering of the single semiconductor element to a carrier board;

wherein at least one side face (33) of the single semiconductor element is at least partly provided with an insulator layer (25) for the avoidance of short circuits on the soldering of the single semiconductor element to the carrier board; and

wherein the solder contacts (29) have different outlines at the contact side (23) of the single semiconductor element.